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☐	L4	(linear$2 near5 (frequency or rate or speed) near5 transition$3)	276
☐	L3	L1 with clock$4	5
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☐	L1	(linear$2 near5 (frequency or rate or speed) near5 transition$3)	194

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L6: Entry 5 of 8 File: USPT Oct 12, 1999

DOCUMENT-IDENTIFIER: US 5964881 A
TITLE: System and method to control microprocessor startup to reduce power supply bulk capacitance needs

Detailed Description Text (4):
The intelligent clock generating system 50 provides the core clock 52 with a clock signal which is used to drive the microprocessor 60. If the microprocessor 60 is operating in an active mode, the intelligent clock generating system 50 provides the core clock with a clock signal having a frequency suitable for driving the microprocessor 60 in the active mode. However, if the microprocessor 60 is transitioning from an idle state to the active state, the intelligent clock generating system 50 provides the core clock 52 with a clock signal having a frequency which provides for gradually increasing the operating speed of the microprocessor 60. More particularly, the intelligent clock generating system 50 generates a clock signal of increasing frequency up to an active state running frequency as the microprocessor 60 is transitioning from the idle state to the active state. The frequency of the microprocessor is increased in a substantially linear or ramped fashion during the transition from the idle state to the active state.

L6: Entry 6 of 8 File: USPT Oct 13, 1998

DOCUMENT-IDENTIFIER: US 5822387 A
TITLE: Apparatus for fast phase-locked loop (PLL) frequency slewing during power on

Detailed Description Text (13):
Although there are various methods for frequency-slewing, in one methodology, frequency-slewing is initiated by "stepping" the PLL input reference signal between frequencies. This stepping of input frequencies occurs during interval D. During this interval, the PLL 12 output frequency transitions from F.sub.1, to F.sub.2, in a fairly linear, relatively slow, controlled fashion, as shown as the transition between points 26, and 27 in FIG. 2A. During interval D, the actual phase error is large, as shown in FIG. 2D. However, lock detector 14 does not change the state of the frequency-slewing enable signal, even though the system is not, technically, phase-locked. Ostensibly, the reason for continuing to assert the enable signal to thereby enable frequency-slewing is to achieve one of the objects of the present invention, which is, namely, to allow a controlled transition between output frequencies. If frequency-slewing were disabled, transition would occur much more quickly, and thus defeat an object of the invention. Further, another object of the invention is to maintain the frequency-slewing mode in an enabled state after the power-up interval has elapsed, and to maintain it until the system is powered off. To achieve these and other objects, the PLL 12 includes circuitry, to be described in greater detail below, for ensuring that the gated out-of-lock indicative signal 22, when in the frequency-slewing mode, is generated to indicate lock within the predetermined error margin associated with lock detector 14 to thereby maintain the enable signal in an active state. The concept involved with this structure, in a charge pump-based preferred embodiment, is to limit the excursion of the UP, and DOWN signals (whose pulse width is indicative of the extent to which the PLL is out-of-lock) such that it appears to the lock detector 14 that the PLL 12 is, in-fact, locked. Limiting the UP/DOWN signals also serves to limit the rate at which the output reference signal varies. Conventional clock chips have been observed to power-up in a time span of no less than approximately 50 milliseconds. A clock synthesizer 10 in accordance with the present invention is characterized by a power-up time on the order of approximately 100 microseconds. This improvement provides advantages in systems having low power requirements.

L6: Entry 8 of 8 File: USPT Dec 23, 1980

DOCUMENT-IDENTIFIER: US 4240318 A
TITLE: Portamento and glide tone generator having multimode clock circuit

Detailed Description Text (7):
As explained in more detail in the previously mentioned application, rate multiplier 34, in association with rate control clock 44, is effective for compensating operation of the tone generator to insure that corresponding musical intervals are linearly swept in equal time intervals. As a result, a given number of musical intervals are swept in a corresponding number of equal time intervals. It has been found that it is often desirable to sweep the output tone signal frequency through one or more musical intervals in an exponential rather than a linear fashion as illustrated by curves 11 and 13 in FIG. 1. Such an exponential sweep has the advantage of producing a less abrupt transition at the end of the sweep since the rate of change of the frequency of the tone signal is substantially less than in the linear case.

L6: Entry 2 of 8 File: PGPB Nov 1, 2001

DOCUMENT-IDENTIFIER: US 20010036239 A1

TITLE: Phase locked loop circuit and method of frequency modulation in phase locked loop circuit

Detail Description Paragraph:

[0059] If the frequency-dividing rate is changed, the frequency of the clock signal generated by the phase locked loop circuit is changed mainly depending upon the transitional characteristic which depends both upon the characteristics of the charge pump circuit 2 and the low pass filter 3 and upon the gain of the voltage control oscillator 4, The variation in frequency of the clock signal upon the change of the frequency-diving rate appears with a transitional delay. If the change between "0" and "1" of the control signal PESL appears so that the next change of the frequency-dividing rate is made before the transitional change in frequency of the clock signal caused by the change of the previous change of the frequency-dividing rate is terminated, then the variation in the frequency of the clock signal is smoothed by the integral effect. The effect is remarkable if the switches are made to the two kinds of the frequency-dividing rates so that the frequency-dividing rates are changed before the first appearing peak in the transitional variation in the frequency of the clock signal. The value of the signal "V" is selected to set the frequency of the change to the frequency-dividing rate made in the one modulation timer period, and the two kinds of the frequency-divided rate are determined so that frequency of the frequency divided pulses are proper value for the transitional characteristics, whereby the frequency of the clock signal shows the linear variation in the form of the triangle waveform. This is common to the second time period corresponding to falling of the modulation waveform In order to emphasize this effect, it is preferable that the transitional characteristics of the phase locked loop circuit is gentle and the locking time period is long and the band width is wide,

L2: Entry 2 of 5 File: USPT Jul 8, 2003

DOCUMENT-IDENTIFIER: US 6590461 B2
TITLE: Frequency conversion apparatus and method

Detailed Description Text (62):
Thus, since a phase shift operation period can be equally distributed as much as possible, a comparison clock signal phase transition characteristic becomes linear, whereby frequency stability of the output signal can be optimized.

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L2: Entry 3 of 5 File: USPT Apr 22, 2003

DOCUMENT-IDENTIFIER: US 6553057 B1
TITLE: Circuit and method for linear control of a spread spectrum transition

CLAIMS:

14. A method of producing a low slew rate linear transition in the turn-on transient response of a spread spectrum clock generator comprising the steps of: (A) generating a sequence of linearity ROM codes according to a predetermined mathematical formula; (B) optimizing said sequence of linearity ROM codes according to one or more predetermined criteria; and (C) modulating a clock signal in response to (i) said sequence of linearity ROM codes and (ii) a command signal.

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1. **Joint wavelet transform and vector quantization for speech coding**
Mandridake, E.; Najim, M.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on
3-6 May 1993 Page(s):699 - 702
AbstractPlus | Full Text: PDF(398 KB) IEEE CNF

2. **Joint wavelet transform and vector quantization for speech coding**
Mandridake, E.; Najim, M.;
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on
3-6 May 1993 Page(s):699 - 702 vol.1
AbstractPlus | Full Text: PDF(268 KB) IEEE CNF

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1. **Modified Booth algorithm for high radix fixed-point multiplication**
Madrid, P.E.; Millar, B.; Swartzlander, E.E., Jr.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 1, Issue 2, June 1993 Page(s):164 - 167
AbstractPlus | Full Text: PDF(368 KB) IEEE JNL

2. **A fast hybrid multiplier combining Booth and Wallace/Dadda algorithms**
Millar, B.; Madrid, P.E.; Swartzlander, E.E., Jr.;
Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on
9-12 Aug. 1992 Page(s):158 - 165 vol.1
AbstractPlus | Full Text: PDF(488 KB) IEEE CNF

3. **Modified Booth algorithm for high radix multiplication**
Madrid, P.E.; Millar, B.; Swartzlander, E.E., Jr.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., International Conference on
11-14 Oct. 1992 Page(s):118 - 121
AbstractPlus | Full Text: PDF(404 KB) IEEE CNF

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1. **Liquid nitrogen CMOS for computer applications**
Gaensslen, F.H.; Meyer, D.D.;
Computer Design: VLSI in Computers and Processors, 1991. ICCD '91. Proceedings., International Conference on
14-16 Oct. 1991 Page(s):4 - 8
AbstractPlus | Full Text: PDF(404 KB) IEEE CNF

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
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1. **Electrodeposited iridium oxide for neural stimulation and recording electrodes**
Meyer, R.D.; Cogan, S.F.; Nguyen, T.H.; Rauh, R.D.;
Neural Systems and Rehabilitation Engineering, IEEE Transactions on [see also IEEE Rehabilitation Engineering]
Volume 9, Issue 1, March 2001 Page(s):2 - 11
AbstractPlus | References | Full Text: PDF(220 KB) IEEE JNL

2. **Feasibility and limitations of the endoscopic instrumentation to release carpal lig**
Tamarapalli, J.R.; Meyer, R.D.;
Biomedical Engineering Conference, 1996., Proceedings of the 1996 Fifteenth Souther
29-31 March 1996 Page(s):157 - 159
AbstractPlus | Full Text: PDF(208 KB) IEEE CNF

3. **Biomechanics of bone-ligament-bone units for reconstruction of the scapholuna**
Moeini, S.R.; Perry, W.; Tamarapalli, J.R.; Lemons, J.E.; Wilkins, M.J.; Meyer, R.D.;
Biomedical Engineering Conference, 1995., Proceedings of the 1995 Fourteenth South
7-9 April 1995 Page(s):98 - 100
AbstractPlus | Full Text: PDF(368 KB) IEEE CNF

4. **A multipurpose endoscopy training apparatus**
Tamarapalli, J.R.; Meyer, R.D.; Lemons, J.E.;
Biomedical Engineering Conference, 1995., Proceedings of the 1995 Fourteenth South
7-9 April 1995 Page(s):297 - 299
AbstractPlus | Full Text: PDF(160 KB) IEEE CNF

5. **Electrodeposition of iridium oxide charge injection electrodes**
Meyer, R.D.; Nguyen, T.H.; Twardoch, U.M.; Rauh, R.D.; Cogan, S.F.;
[Engineering in Medicine and Biology, 1999. 21st Annual Conf. and the 1999 Annual F
Biomedical Engineering Soc.] BMES/EMBS Conference, 1999. Proceedings of the Firs
Volume 1, 13-16 Oct. 1999 Page(s):382 vol.1
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